REMARKS

This paper is in response to the Office Action mailed on 12/12/2005. In the Office Action, (i) claims 1-8, 10-12, 21-24, 26-28 were rejected under 35 USC 102(e); (ii) claims 13 and 29 were rejected under 35 USC 103(a); (iii) claims 9, 25, 15-20, 30, and 31-34 were objected for being dependent upon a rejected base claim; and (iv) the drawing of Figure 1 was objected.

Reexamination and reconsideration is respectfully requested in view of the amendments and the remarks made herein.

Applicant has amended claims 1-15, 21, 23, and 29-31 by this response. New dependent claim 35 has been added. No claim has been cancelled. Accordingly, claims 1-35 are now pending.

Of the pending claims, claims 1, 5, 15, 21, and 31 are independent claims.

Applicant believes that no new matter has been added by this response.

I) Drawing Objection and Amendments

The Examiner has objected to drawing of Figure 1 for missing the legend "PRIOR ART".

Applicant has amended the drawing of Figure 1 to include the legend "PRIOR ART" as indicated in Appendix I.

Applicant believes that this objection to the drawing of Figure 1 is now moot and respectfully requests its withdrawal.

Applicant has further amended the drawing of Figure 1 to change the output of the latched labeled "Q" to --L-- to be consistent with the use of the latch output label used in other Figures and the detailed description.

Applicant has amended the drawing of Figure 6A to include the word --NO-- next to the decision block 616 as the obvious alternative choice to "YES".

Applicant has amended the drawing of Figure 6C to correct a typographical error in the decision block 682 of the word "TIME".

Applicant respectfully submits that no new matter has been added by these amendments to the drawings.

Clean drawing sheets including Figures 1, 6A, and 6C as amended are attached hereto as Appendix 1.

II) Claim Objections

In section 16 of the Office Action, claims 9, 25, 15-20, 30, and 31-34 were objected for being dependent upon a rejected base claim. The Office Action indicated that these claims would be allowable if rewritten into independent form.

Claims 15 and 31 have been rewritten into independent form including the base claim and any intermediate claim. Claims 16-20 and 32-34 depend directly or indirectly from independent claims 15 and 31 respectively. Accordingly, Applicant respectfully submits that this objection is moot as to claims 15-20 and 31-34 and respectfully requests its withdrawal.

Dependent claims 9, 25, and 30 depend from independent claims 1 and 21. For the reasons that follow below, Applicant respectfully submits that independent claims 1 and 21 and these respective dependent claims 9, 25, and 30 are in condition for allowance.

Applicant respectfully requests the withdrawal of the objection to claims 9, 25, 15-20, 30, and 31-34.

III) Claim Rejections Under 35 U.S.C. 102(e)

In sections 5-12 of the Office Action, claims 1-8, 10-12, 21-24, and 26-28 were rejected under 35 U.S.C. § 102(e) as being anticipated by US patent application publication 2003/0154433 filed by Wang et al. ("Wang"). Applicant respectfully traverses this rejection.

Applicant has amended independent claims 1, 5, and 21.

Regarding independent claims 1 and 21, the Office Action alleges in section 6 that Wang teaches "a design method for transforming sequential logic design into equivalent combinational logic (Fig. 2, 17-19, summary) comprising simulating each stage of a clocking sequence to produce simulation values and saving the simulation values and performing a plurality of backward logic traces based on the saved simulation value to provide an equivalent combinational logic representation of sequential logic design (0011 describes that the invention is used to generated a broadcast scan patterns that are applied to the scan cells (memory elements) of an 1C design under test. This process converts the virtual scan patterns stored in an ATE into broadcast scan patterns that are applied to the package scan input pins of the 1C using a broadcaster. The broadcast maps the virtual scan patterns into their corresponding broadcast scan patterns that are used to test for various faults, such as stuck-at faults, delay faults, and bridging faults in an 1C. The ATE performs simulation to produce and storing simulation values. Backtracking logic traces on any shift clock cycle is described in 0015. Figs. 17-19 show a transform model that transforms a sequential logic design into an equivalent combinational circuit. 0013 describes combinational equivalent circuit)." Applicant respectfully disagrees.

Regarding independent claim 5, the Office Action alleges in section 7 that Wang teaches "a design method for transforming sequential logic design into equivalent combinational logic (Figs. 2, 17-19, summary) comprising simulating each stage of a clocking sequence to produce simulation values and saving the simulation values and performing a plurality of backward logic traces based on the saved simulation value to provide an equivalent combinational logic representation of sequential logic design (0011 describes that the invention is used to generated a broadcast scan patterns that are applied to the scan cells (memory elements) of an 1C design under test. This process converts the virtual scan patterns stored in an ATE into broadcast scan patterns that are applied to the package scan input pins of the 1C using a broadcaster. The broadcast maps the virtual scan patterns into their corresponding broadcast scan patterns that are used to test for various faults, such as stuck-at faults, delay faults, and bridging faults in an 1C. The ATE performs simulation to produce and storing simulation values. Backtracking logic traces on any shift clock cycle is described in 0015. Figs. 17-19 show a transform model that transforms a sequential logic design into an equivalent combinational circuit). In addition, Wang

et al. teach simulation a scan operation (generation of broadcast scan patterns, at least see 0014)." Applicant respectfully disagrees.

The Office Action alleges that Wang's "ATE performs simulation to produce and storing simulation values." However, Wang only discloses fault simulation on a combinational circuit model. As illustrated in Wang's Figure 18, after Wang's combinational circuit model 1806, "combinational fault simulation 1807 is performed, if so required, for a number of random patterns and all detected faults are removed from the fault list." [Wang, paragraph 0096].

That is, Wang does not disclose "simulating each stage of a clocking sequence ***on a sequential logic design*** to produce simulation values" as is recited in amended independent claims 1, 5, and 21. (emphasis added)

The Office Action alleges that "Backtracking logic traces on any shift clock cycle is described in 0015" of Wang. Applicant respectfully disagrees. Wang's paragraph [0015] generally describes Wang's "broadcast scan chain reordering step" by reordering scan cell outputs so that "only one constrained scan cell is located on a single broadcast channel during any shift clock cycle". Wang's input cone analysis is from each "scan cell input" to all "scan cell outputs". Moreover, Wang's input cone analysis 1707 step illustrated in Wang's Figure 17 is performed with the combinational circuit model 1706.

Wang does not disclose "performing a plurality of ***backward logic traces on the sequential logic design***" as is recited in the amended independent claims 1, 5, and 21. (emphasis added)

The Office Action further alleges that Wang's "Figs. 17-19 show a transform model that transforms a sequential logic design into an equivalent combinational circuit". However, there is no description in Wang of the transformation blocks 1705 and 1805 illustrated respectively in Wang's Figures 17-18. The general statement in Wang's paragraph's [0095] and [0096] do not disclose how a sequential circuit model 1704,1804 may be transformed into a combinational circuit model 1706,1806.

Specifically, Wang does not disclose "performing a plurality of backward logic traces on the sequential logic design based on the saved simulation values to provide an equivalent combinational logic representation of the sequential logic design" as is recited in amended independent claims 1, 5, and 21.

The Office Action further alleges that "Wang et al. teach simulation [of] a scan operation (generation of broadcast scan patterns, at least see 0014)". Applicant respectfully disagrees. As discussed previously, Wang only discloses fault simulation on a combinational circuit model. As illustrated in Wang's Figure 18, after Wang's combinational circuit model 1806, "combinational fault simulation 1807 is performed, if so required, for a number of random patterns and all detected faults are removed from the fault list." [Wang, paragraph 0096].

Wang does not disclose "simulating a scan operation on the sequential logic design" as is recited in amended independent claim 5.

For the foregoing reasons, Applicant respectfully submits that independent claims 1, 5, and 21 are not anticipated by Wang.

Dependent claims 2-4 and 8-12, 14 depend directly or indirectly from independent claim 1. Dependent claims 6-7 depend directly or indirectly from independent claim 5. Dependent claims 22-30 depend directly or indirectly from independent claim 21.

Applicant believes that independent claims 1, 5, and 21 are in condition for allowance over the cited prior art such that dependent claims depending respectively there-from with added limitations are also in condition for allowance. Applicant respectfully submits that dependent claims 2-4, 6-7, 8-12, 14, and 22-30 are also in condition for allowance over the cited prior art.

Accordingly, Applicant respectfully requests the withdrawal of the 35 USC 102(e) rejection of claims 1-8, 10-12, 21-24, and 26-28 over US patent application publication 2003/0154433 filed by Wang et al. ("Wang").

IV) Claim Rejections Under 35 U.S.C. § 103(a)

In sections 14-15 of the Office Action, claims 13 and 29 were rejected under 35 U.S.C. § 103(a) as being obvious over Wang in view of US pat. No. 5,878,055 issued to David Howard Allen ("Allen"). Applicant respectfully traverses.

The remarks above with respect to independent claims 1 and 21 are incorporated here by reference. Applicant respectfully submits that independent claims 1 and 21 are not made obvious over the combination of Wang and Allen.

Claim 13 depends directly from independent claim 1. Claim 29 depends directly from independent claim 21.

Applicant believes that independent claims 1 and 21 are in condition for allowance over the cited prior art such that dependent claims 13 and 29 depending respectively there-from with added limitations are also in condition for allowance. Applicant respectfully submits that dependent claims 13 and 29 are also in condition for allowance over the cited prior art.

Accordingly, Applicant respectfully requests the withdrawal of the 35 USC 103(a) rejection of claims 13 and 29 over the combination of US patent application publication 2003/0154433 filed by Wang and US pat. No. 5,878,055 issued to Allen.

V) New Claim

Applicant has added new claim 35.

New claim 35 depends directly from independent claim 1. Applicant believes it has placed independent claim 1 in condition for allowance such that dependent claim 35 depending there-from with further limitations is also in condition for allowance.

Applicant respectfully submits that new claim 35 is in condition for allowance with independent claim 1.

VI) Claim Amendments

Applicant has amended claims 1-15, 21, 23, and 29-31.

As discussed previously, claims 15 and 31 were amended into independent claim form.

Independent claims 1, 5, and 21 were amended to simplify their preambles and to clarify the claimed invention in that the elements of "simulating each stage of a clocking sequence to produce simulation values" and "performing a plurality of backward logic traces based on the saved simulation values to provide an equivalent combinational logic representation" were performed on a sequential logic design.

Independent claim 5 was further amended to clarify the claimed invention in that the element of "simulating a scan operation" was a part of the "simulating each stage of a clocking sequence to produce simulation values" and was performed on a sequential logic design.

Dependent claims 2-4, 6-14 were amended to simplify their preambles in accordance with the amendment to the preambles of independent claims 1 and 5.

Dependent claims 13 and 29 were amended to include the word "logic" to be consistent with the phrase "sequential logic design" used in independent claims 1 and 21 from which they respectfully depend.

Dependent claims 14 and 30 were further amended to clarify the claimed invention in that the method element of "saving distinct states in response to the one or more chopped clocks".

Dependent claim 10 was further amended to clarify the claimed invention in that the equivalent combinational logic representation facilitates automatic test pattern generation and to recite a further method element of "mapping test patterns back to the sequential logic design".

Dependent claim 7 was further amended to clarify the claimed invention in that the element of "turning off all clocks" is for "the simulating of the scan operation".

Dependent claims 3-4, 6-9, 11, 23, were further amended to include punctuation, such as a comma or colon.

Applicant believes that the foregoing claim amendments have been made to clarify the claimed invention, unrelated to reasons of patentability.

VII) Specification Amendments

Applicant has amended paragraph nos. [0027], [0035], [0045], [0055], and [0072].

Paragraph no. [0027] was amended to add the letter --L-- to be consistent with the use of "L" as a latch output elsewhere in the specification and the drawing amendment of Figure 1.

Paragraph no. [0035] was amended to amended to add the word --sequential-- to clarify that the circuit 400 is an "exemplary sequential circuit" to be consistent with its description elsewhere in the specification.

Paragraph no. [0045] was amended to remove a typographical error, a comma.

Paragraph no. [0055] was amended to correct a grammar error changing "precede" to --precedes--.

Paragraph no. [0072] was amended to correct a typographical error, capitalization of the letter "E" in the word --even--.

Applicant respectfully submits that no new matter has been added by these amendments to the specification.

CONCLUSION

In view of the foregoing, reconsideration of the rejections and objections is respectfully requested. Allowance of the claims is respectfully solicited.

The Examiner is invited to contact Applicant's undersigned counsel by telephone at (714) 557-3800 to expedite the prosecution of this case should there be any unresolved matters remaining.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. If any other petition is necessary for consideration of this paper, it is hereby so petitioned. Please charge any shortage in fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 02-2666 and please credit any excess fees to such deposit account.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 *on:* June 12, 2006.

Colette Angle 6/12/06

Colette Angle *Date*

Appendix I

CLEAN DRAWING SHEETS

FIGURES 1, 6A, and 6C